RECEIVED
CENTRAL FAX CENTER
JUN 13 2007

REMARKS

Claims 1-11 and 13-33 are pending. Claim 11 is amended herein and claim 12 is cancelled. Claims 1-2, 4, 10, 11, 14, 15, 18, 19, 23, 24, 25, 28, and 33 stand rejected in the Office Action as being allegedly unpatentable over Yong, Lian, *FPGA Implementation of High Speed Multiplierless Frequency Response Masking FIR Filters*, October 2000, IEEE Workshop on Signal Processing Systems, pages 317 – 325, (hereafter "Lian") in view of Young-Ho Lee et al. *GA-Based Design of Multiplierless 2-D Digital Filters with Very Low Roundoff Noise*, November 1996, Proceedings of IEEE Asia Pacific Conference on Circuits and Systems, pages 223-226 (hereafter "Lee"). For the Examiner's convenience and reference, Applicant's remarks are presented in the order in which the corresponding issues were raised in the Office Action. In view of the following remarks, Applicant respectfully requests reconsideration of all pending claims.

Rejections under 35 U.S.C. § 103(a)

Claims 1-2, 4, 10, 11, 14, 15, 18, 19, 23, 24, 25, 28, and 33 stand rejected in the Office Action as being allegedly unpatentable under 35 U.S.C. § 103(a) over Lian in view of Lee. A rejection under § 103 requires that, "all of the claim limitations must be taught or suggested by the prior art." *In re Royka*, 490 F.2d 981 (CCPA 1971); *also see* MPEP § 2143.03. At the outset, Applicants point out that neither Lian nor Lee disclose a 1-D Infinite Impulse Response (IIR) filter as claimed in the Application; Lian discusses finite impulse response filter (FIR) and Lee discusses a 2-D IIR filter. However, even if a 1-D IIR filter were added to the alleged teachings of Lian and Lee, Applicants

respectfully traverse the rejection of claims 1-2, 4, 10, 11, 14, 15, 18, 19, 23, 24, 25, 28, and 33 since, even in combination, Lian and Lee fail to teach or suggest at least one of the limitations of these claims.

Independent Claims 1 and 18 recite, "... a first shift register having an input to receive input samples; a second shift register having an input to receive previous samples..." *See* Claim 1, 18; emphasis added. Independent Claim 11, recites, "receiving input samples representative of the input signal and previous outputs, wherein receiving the input samples and previous outputs includes storing the input samples in a first shift register and storing the previous outputs in a second shift register." *See* Claim 11 as amended herein, emphasis added. Claim 24 recites, "shift register means for receiving the input samples and previous outputs." *See* Claim 24; emphasis added. Neither Lee nor Lian teaches an infinite impulse response filter incorporating shift registers as recited in Claims 1, 18, 11, and 24. The Office Action purports that Lian teaches such shift registers by way of a, "dual port RAM." However, a RAM (random access memory) is not a shift register as recited in the claims. A shift-register is an aggregation of one or more "flip-flop" circuit elements; "shift registers are normally implemented by means of *D, S-R or J-K* flip-flops ." Richard C. Dorf et al., *The Electrical Engineering Handbook, 2nd Ed., CRC Press*, 1997. By contrast, a RAM is not built from flip-flop components or circuitry, but is typically embodied as a separate, randomly accessible (i.e., randomly addressable) circuitry. *See The Electrical Engineering Handbook,* at 1805-1813.

Moreover, Liam teaches away from the use of flip-flops as a delay element as recited in the claims. When used as the basis of an obviousness rejection, a prior art

reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. See *W.L. Gore & Associates, Inc., v. Garlock, Inc.*, 721 F.2d 1540, 220 (Fed. Cir. 1983); Also see MPEP § 2141.03. Lian teaches away from the use of a shift register and/or flip-flops in the filter allegedly disclosed therein; Lian states that, "... it is not economic to use flip-flops [shift registers] to implement delay elements .. [cites deficiencies with flip flops available on FPGAs] ... it is more efficient to use RAM to implement delay elements .." Lee pg. 322.

Since Neither Lian nor Lee teach or suggest the use of a shift register having an input to receive input samples or a shift register having an input to receive previous outputs, Applicants respectfully traverse the rejection of Claims 1, 11, 18, and 24. In addition, Applicants respectfully traverse the rejection of Claims 2-10, 13-17, and 19-23, and 25-33 since, if an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988); *also see* MPEP § 2143.03.

General Considerations

By the remarks provided herein, Applicant has addressed all outstanding issues presented in the Office Action. Applicant notes that the remarks presented herein have been made merely to clarify the claimed invention from elements purported by the Office Action to be taught by the cited reference. Such remarks should not be construed as acquiescence, on the part of Applicant, as to the purported teachings or prior art status of the cited reference, nor as to the characterization of the cited reference advanced in the Office Action. Accordingly, Applicant reserves the right to

challenge the purported teachings and prior art status of the cited reference at an appropriate time.

CONCLUSION

For the reasons discussed above, Applicant submits that the claims are in proper condition for allowance, and a Notice of Allowance is respectfully requested. If the Examiner notes any further matters that may be resolved by a telephone interview, the Examiner is encouraged to contact John Thompson by telephone at (801)-578-6994

DATED this 13 day of June, 2007.

Respectfully submitted,

John R. Thompson
Registration No. 40,842